Claims

What is claimed is:

1. A system for regulating gate oxide layer formation in semiconductor devices, comprising:

a first stacked gate oxide sublayer former operative to form one or more gate oxide layers on a portion of a wafer;

a second stacked gate oxide sublayer former operative to form one or more gate oxide layers on a portion of a wafer;

a first gate oxide sublayer former driving system for driving the first gate oxide sublayer former;

a second gate oxide sublayer former driving system for driving the second gate oxide sublayer former;

a system for directing light to the portion of the wafer;

a system for collecting light reflected from the portion of the wafer;

a measuring system for measuring parameters of gate oxide formation thickness and/or uniformity based on collected light reflected from one or more gate oxide formations; and

a processor operatively coupled to the measuring system and the gate oxide former driving system, the processor receiving gate oxide formation thickness and/or uniformity data from the measuring system and the processor using the data to at least partially base control of the at least one gate oxide former so as to regulate gate oxide thickness and/or uniformity on the portion of the wafer.

2. The system of claim 1, wherein the thickness of the first stacked gate oxide sublayer is between 20 and 0.1 nanometers.

3. The system of claim 1, wherein the thickness of the second stacked gate oxide sublayer is between 20 and 0.1 nanometers.

4. The system of claim 1, wherein the thickness of the first stacked gate oxide sublayer is less than about 20 nanometers.

5. The system of claim 1, wherein the thickness of the second stacked gate oxide sublayer is less than about 20 nanometers.

6. The system of claim 1, the measuring system further including a scatterometry system for processing the light reflected from the one or more gate oxide layer formations.

7. The system of claim 1, where the gate oxide layer is a high K material.

8. The system of claim 1, where the gate oxide layer is a metal oxide.

9. The system of claim 6, the processor being operatively coupled to the scatterometry system, the processor analyzing data relating to thickness and/or uniformity received from the scatterometry system, and the processor basing control of the at least one gate oxide former at least partially on the analyzed data.

10. The system of claim 8, the processor being operatively coupled to the scatterometry system, the processor analyzing data relating to thickness and/or uniformity received from the scatterometry system, and the processor basing control of the at least one gate oxide former at least partially on the analyzed data.

11. The system of claim 1, the processor mapping the wafer into a plurality of grid blocks, and making a determination of gate oxide layer formation thickness and/or uniformity at a grid block.

12. The system of claim 1, wherein the processor determines the existence of an unacceptable gate oxide thickness and/or uniformity for at least a portion of the wafer based upon the determined thickness differing from an acceptable value.

13. The system of claim 12, wherein the processor controls the at least one gate oxide former to regulate gate oxide layer formation on the at least one portion to an acceptable value.

14. A method for regulating gate oxide layer formation, comprising:

defining a wafer as a plurality of portions;

establishing one or more gate oxide layer formations to be formed;

directing light onto at least one of the gate oxide layer formations;

collecting light reflected from at least one gate oxide layer formation;

analyzing the reflected light to determine thickness and/or uniformity of the at least one gate oxide layer formation; and

controlling one or more gate oxide layer formers to regulate gate oxide formation of the at least one gate oxide layer formation.

15. The method of claim 14, wherein analyzing the reflected light further comprises:

employing a scatterometry system to process the reflected light.

16. The method of claim 14, where the gate oxide layer is a high K material.

17. The method of claim 14, where the gate oxide layer is a metal oxide.

18. The method of claim 14, further comprising:

using a processor to control the at least one gate oxide former based at least partially on data received from the scatterometry system.

19. The method of claim 18, further comprising:

using a processor to control the at least one gate oxide former based at least partially on data received from the scatterometry system.

20. A method for regulating gate oxide layer formation, comprising:

partitioning a wafer into a plurality of grid blocks;

using one or more gate oxide layer formers to form one or more gate oxide layers on the wafer, each gate oxide former functionally corresponding to a respective grid block;

determining thickness and/or uniformity of the one or more gate oxide layer formations on one or more portions of the wafer, each portion corresponding to a respective grid block; and

using a processor to coordinate control of the gate oxide layer formers, respectively, in accordance with determined gate oxide thickness and/or uniformity of the respective portions of the wafer.

21. A system for regulating gate oxide layer formation, comprising:

first sensing means for sensing gate oxide layer formation thickness of one or more of gate oxide layers;

second sensing means for sensing uniformity of one or more of gate oxide layer formations;

forming means for forming one or more gate oxide layers; and

controlling means for selectively controlling the forming means so as to regulate gate oxide formation.